AMENDMENTS TO THE SPECIFICATION

Please replace paragraph [1001] with the following amended paragraph:

[1001] This application is related to co-pending U.S. Application No. 10/729,831 ~~xx/xxx,xxx (Attorney Docket No. 023-0028)~~ by En-Hsing Chen, et al, entitled "NAND Memory Array Incorporating Capacitance Boosting of Channel Regions in Unselected Memory Cells and Method for Operation of Same," filed on even date herewith, which application is hereby incorporated by reference in its entirety; and to co-pending U.S. Application No. 10/729,844 ~~xx/xxx,xxx (Attorney Docket No. 023-0030)~~ by En-Hsing Chen, et al, entitled "NAND Memory Array Incorporating Multiple Write Pulse Programming of Individual Memory Cells and Method for Operation of Same," filed on even date herewith, which application is hereby incorporated by reference in its entirety; and to co-pending U.S. Application No. 10/729,843 ~~xx/xxx,xxx (Attorney Docket No. 023-0031)~~ by Luca G. Fasoli, et al, entitled "Memory Array Incorporating Memory Cells Arranged in NAND Strings," filed on even date herewith, which application is hereby incorporated by reference in its entirety.

Please replace paragraph [1043] with the following amended paragraph:

[1043] In a preferred embodiment, the memory cell devices and block select devices are both SONOS devices which are implanted to shift the thermal equilibrium (i.e., minimum trapped negative charge in the nitride) threshold voltage V_T to depletion mode. A depletion mode implant that is a slow diffuser, preferably antimony or arsenic, is preferably used because of the relatively higher diffusion of such dopants in a polycrystalline layer compared with a crystalline substrate, and also due to the extremely small dimensions of the devices. The erased state V_T is substantially depletion mode, preferably -2V to -3V threshold, while the programmed state V_T is preferable about zero volts. The memory cells are programmed or erased to one of the two threshold voltages according to the data state, but the block select devices are preferably programmed to have about a one-volt threshold voltage and maintained in this programmed state. Suitable fabrication methods are described in U.S. Application No. 10/335,089 ~~(Attorney Docket No. 023-0020)~~ by Andrew J. Walker, et al, entitled "Method for Fabricating Programmable

Memory Array Structures Incorporating Series-Connected Transistor Strings," filed on December 31, 2002, which application is hereby incorporated by reference in its entirety.

Please replace paragraph [1086] with the following amended paragraph:

[1086] As shown in Figs. 17A, 17B, 17D, and 17E, compact arrangements of zias in a straight line are preferred to save area for the contacts to the global bit lines. This is especially advantageous for the non-mirrored arrangement of NAND strings shown in Figs. 17A, 17B and 17C. Any known processing technique for producing zias at a very tight spacing of the NAND channel regions can be used in combination with the NAND string arrangements shown in Figs. 17A, 17B, 17D, and 17E. In Fig 17A the non-mirrored NAND strings are connected to global bit lines on a single layer below the memory lines and coincident with the memory lines so they do not appear in the Fig 17A plan view. Alternatively, zia 1701 could connect to global bit lines on one layer while adjacent zia 1702 could connect to global bit line on a second global bit line layer. A vertically overlapping zia technique that forms a zia connection from a common memory level to two wiring levels may be used advantageously to connect the NAND strings to global bit lines on two layers, as shown in arrangement 17B. Such vertically overlapping zia techniques are described in more detail in U.S. Patent Application No. 10/728,451 ~~xx/xxx,xxx, (Attorney Docket No. MA-112)~~ by Roy E. Scheuerlein, et al., entitled "High Density Contact to Relaxed Geometry Layers," filed on even date herewith, which application is hereby incorporated by reference in its entirety. The two global bit line layers can both be below the memory array or both above the memory array. In Fig 17C, the zia locations are staggered to enlarge the spacing between the zia holes and in some embodiments provide for a pad region on the NAND string channel layers and global bit line layers. The use of in-line zias (as shown in Fig. 24, Fig. 25, and Fig. 28 of "Method for Fabricating Programmable Memory Array Structures Incorporating Series-Connected Transistor Strings," referenced above) can also provide a tighter spacing of zias in the arrangements shown in Figs. 17A, 17B, 17D, or 17E, while connecting the zia to a NAND string in a selected block and a NAND string in an adjacent block. Multi-layer vertical zia holes (as shown in Fig. 29 of "Method for Fabricating Programmable Memory Array Structures Incorporating Series-Connected Transistor Strings," referenced above) form compact zias which are also suitable for each of these arrangements.

Please replace paragraph [1110] with the following amended paragraph:

[1110] While any of a variety of semiconductor processes may be advantageously utilized to fabricate memory arrays having NAND strings, many embodiments described above contemplate memory cells formed as thin film transistors above a semiconductor substrate. Preferred methods for fabricating such memory arrays are described in: U.S. Application No. 10/334,649 ~~(Attorney Docket No. MA-087)~~, filed on December 31, 2002, by Andrew J. Walker, et al., entitled "Formation of Thin Channels for TFT Devices to Ensure Low Variability of Threshold Voltages," which application is hereby incorporated by reference; U.S. Application No. 10/079,472, filed on February 19, 2002, by Maitreyee Mahajani, et al., entitled "Gate Dielectric Structures for Integrated Circuits and Methods for Making and Using Such Gate Dielectric Structures," which application is hereby incorporated by reference; U.S. Application No. 10/335,089 ~~(Attorney Docket No. 023-0020)~~ by Andrew J. Walker, et al, entitled "Method for Fabricating Programmable Memory Array Structures Incorporating Series-Connected Transistor Strings," filed on December 31, 2002, which application is hereby incorporated by reference in its entirety; and U.S. Application No. 10/668,693 by Maitreyee Mahajani, et al, entitled "Storage Layer Optimization of a Non Volatile Memory Device," filed on September 23, 2003, which application is hereby incorporated by reference in its entirety. Other useful fabrication methods are described in U.S. Patent Application No. 10/728,437 ~~xx/xxx,xxx, (Attorney Docket No. MA-110)~~ by James M. Cleeves, et al., entitled "Optimization of Critical Dimensions and Pitch of Patterned Features In and Above a Substrate," filed on even date herewith, which application is hereby incorporated by reference in its entirety, and described in U.S. Patent Application No. 10/728,436 ~~xx/xxx,xxx, (Attorney Docket No. MA-111)~~ by Yung-Tin Chen, entitled "Photomask Features with Interior Nonprinting Window Using Alternating Phase Shifting," filed on even date herewith, which application is hereby incorporated by reference in its entirety.

Please replace paragraph [1120] with the following amended paragraph:

[1120] It should be appreciated that the various bias voltages described herein, including negative voltages and high-voltage programming and erase voltages, may be received from external sources, or may be generated internally using any of a number of suitable techniques. It

should also be appreciated that the designations top, left, bottom, and right are merely convenient descriptive terms for the four sides of a memory array. The word lines for a block may be implemented as two inter-digitated groups of word lines oriented horizontally, and the global bit lines for a block may be implemented as two inter-digitated groups of global bit line oriented vertically. Each respective group of word lines or global bit lines may be served by a respective decoder/driver circuit and a respective sense circuit on one of the four sides of the array. Suitable row and column circuits are set forth in "Multi-Headed Decoder Structure Utilizing Memory Array Line Driver with Dual Purpose Driver Device," U. S. Patent Application No. 10/306,887, filed November 27, 2002 ~~(Attorney Docket No. 023-0015)~~, and in "Tree Decoder Structure Particularly Well Suited to Interfacing Array Lines Having Extremely Small Layout Pitch," U. S. Patent Application Serial No. 10/306,888, filed November 27, 2002 ~~(Attorney Docket No. 023-0016)~~, which applications are hereby incorporated by reference in their entirety. The global bit line may be driven by a bit line driver circuit, which may be either directly coupled to the global bit line or may be shared among several global bit lines and coupled by decoding circuitry to a desired global bit line. Suitable driver and decoder circuits are well known in the art.